

AMENDMENTS TO THE CLAIMS:

Claims 1-150 (canceled)

1 ~~151.~~ (previously presented) A synchronous memory device
2 including an array of memory cells, the synchronous memory
3 device comprises:
4 clock receiver circuitry to receive an external clock signal;
5 input receiver circuitry to sample a first operation code in
6 response to a rising edge transition of the external clock signal;
7 a programmable register to store a value which is
8 representative of an amount of time to transpire before the memory
9 device outputs data, wherein the memory device stores the value in
10 the programmable register in response to the first operation code;
11 and
12 output driver circuitry to output data in response to a second
13 operation code, wherein the data is output after the amount of time
14 transpires, and wherein:
15 the output driver circuitry outputs a first portion of
16 the data synchronously with respect to a rising edge
17 transition of the external clock signal and outputs a second
18 portion of the data synchronously with respect to a falling
19 edge transition of the external clock signal.

2
1 ~~152~~. (previously presented) The memory device of claim ~~151~~¹
2 wherein the first operation code is included in a control register
3 access packet.

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1 ~~153~~. (previously presented) The memory device of claim ~~152~~²
2 wherein the first operation code and the value are included in the
3 same control register access packet.

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1 ~~154~~. (previously presented) The memory device of claim ~~151~~¹
2 wherein the memory device is a synchronous dynamic random access
3 memory.

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1 ~~155~~. (previously presented) The memory device of claim ~~151~~¹
2 wherein the input receiver circuitry receives the second operation
3 code and address information.

6
1 ~~156~~. (previously presented) The memory device of claim ~~155~~⁵
2 wherein the input receiver circuitry receives the second operation
3 code and the address information on consecutive clock cycles of the
4 external clock signal.

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1 ~~157~~. (previously presented) The memory device of claim ~~151~~¹
2 wherein the amount of time is a number of clock cycles of the
3 external clock signal.

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1 ~~158~~. (previously presented) The memory device of claim ~~151~~
2 wherein the input receiver circuitry receives a third operation
3 code, wherein the third operation code initiates a write operation
4 in the memory device.

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1 ~~159~~. (previously presented) The memory device of claim ~~158~~
2 wherein the input receiver circuitry receives the third operation
3 code and address information.

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1 ~~160~~. (previously presented) The memory device of claim ~~151~~
2 further including delay lock loop circuitry coupled to the clock
3 receiver circuitry to generate a first internal clock signal,
4 wherein the data is output in response to the first internal clock
5 signal.

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1 ~~161~~. (previously presented) The memory device of claim ~~151~~
2 wherein the output driver circuitry outputs the data onto a bus.

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1 ~~162~~. (previously presented) The memory device of claim ~~161~~
2 wherein the bus includes a set of signal lines to carry multiplexed
3 address information, data and control information.

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1 ~~163~~. (currently amended) A method of operation of a
2 synchronous memory device, wherein the memory device includes an
3 array of memory cells and a programmable register, the method of
4 operation of the memory device comprises:
5 sampling a first operation code synchronously with respect to
6 an external clock signal;
7 receiving a binary value ~~which~~ that is representative of an
8 amount of time to transpire before the memory device outputs data
9 in response to a second operation code, wherein the memory device
10 stores the binary value in the programmable register in response to
11 the first operation code;
12 sampling the second operation code; and
13 outputting the data after the amount of time transpires,
14 wherein a first portion of the data is output synchronously with
15 respect to a first transition of the external clock signal and a
16 second portion of the data is output synchronously with respect to
17 a second transition of the external clock signal.

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1 ~~164~~. (previously presented) The method of claim ~~163~~ ¹³ wherein
2 the second operation code is sampled synchronously with respect to
3 the external clock signal.

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1 ~~165~~. (previously presented) The method of claim ~~163~~ ¹³ wherein
2 the binary value is representative of a number of clock cycles of
3 the external clock signal.

1 ¹⁶~~166~~. (currently amended) The method of claim ¹⁵~~165~~ further
2 including:
3 receiving block size information, wherein the block size
4 information defines an amount of data to be output in response to
5 the second operation code, wherein the memory device outputs the
6 amount of data after the number of clock cycles of the external
7 clock signal transpire.

1 ¹⁷~~167~~. (previously presented) The method of claim ¹³~~163~~ further
2 including receiving address information synchronously with respect
3 to the external clock signal.

1 ¹⁸~~168~~. (currently amended) The method of claim ¹⁷~~167~~ ~~163~~ wherein
2 the address information and the second operation code are included
3 in a read request packet.

1 ¹⁹~~169~~. (previously presented) The method of claim ¹³~~163~~ further
2 including receiving precharge information.

1 ²⁰~~170~~. (previously presented) The method of claim ¹⁹~~169~~ wherein
2 the precharge information includes a binary bit, wherein, after
3 accessing the data from the array of memory cells, the memory
4 device retains contents of a plurality of sense amplifiers for a
5 subsequent memory operation as a result of a first state of the
6 binary bit.

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1 ~~171~~. (previously presented) The method of claim ~~163~~ wherein
2 the first transition of the external clock signal is a rising edge
3 transition and the second transition of the external clock signal
4 is a falling edge transition.

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1 ~~172~~. (previously presented) The method of claim ~~171~~ wherein
2 the first and second transitions of the external clock signal are
3 consecutive transitions of the external clock signal.

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1 ~~173~~. (previously presented) The method of claim ~~163~~ wherein
2 the first operation code is sampled during an initialization
3 sequence after power is applied to the memory device.

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1 ~~174~~. (previously presented) The method of claim ~~163~~ wherein
2 the memory device outputs the data onto an external bus.

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1 ~~175~~. (previously presented) The method of claim ~~174~~ wherein
2 the external bus includes a set of signal lines to carry
3 multiplexed address information, data and control information.

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1 ~~26~~. (previously presented) A method of controlling a
2 synchronous memory device by a memory controller, wherein the
3 memory device includes an array of memory cells and a programmable
4 register, the method of controlling the memory device comprises:
5 providing a first operation code to the memory device, wherein
6 the first operation code initiates an access of the programmable
7 register in the memory device in order to store a binary value;
8 providing the binary value to the memory device, wherein the
9 memory device stores the binary value in the programmable register
10 in response to the first operation code;
11 providing a second operation code to the memory device,
12 wherein the second operation code instructs the memory device to
13 accept data that is issued by the memory controller;
14 providing a first portion of the data to the memory device in
15 response to a rising edge transition of the external clock signal;
16 and
17 providing a second portion of the data to the memory device in
18 response to a falling edge transition of the external clock signal.

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1 ~~27~~. (previously presented) The method of claim 26 wherein
2 the binary value is representative of a delay time to transpire
3 before the memory device samples the data, and wherein the first
4 portion of the data is provided to the memory device after the
5 delay time transpires.

1 ²⁸~~178~~. (previously presented) The method of claim ²⁶~~176~~ wherein
2 the binary value is representative of a number of clock cycles of
3 the external clock signal to transpire before the memory device
4 samples the data, and wherein the first portion of the data is
5 provided to the memory device after the number of clock cycles
6 transpire.

1 ²⁹~~179~~. (previously presented) The method of claim ²⁶~~176~~ wherein
2 the binary value is representative of a delay time to transpire
3 before the memory device outputs data in response to an operation
4 code which instructs the memory device to output data.

1 ³⁰~~180~~. (previously presented) The method of claim ²⁶~~176~~ further
2 including:
3 providing block size information to the memory device, wherein
4 the block size information defines an amount of data to be accepted
5 by the memory device in response to the second operation code.

1 ³¹~~181~~. (previously presented) The method of claim ²⁶~~176~~ further
2 including providing address information to the memory device.

1 ³²~~182~~. (previously presented) The method of claim ³¹~~181~~ wherein
2 the address information and the second operation code are included
3 in a write request packet.

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1 ~~183~~. (previously presented) The method of claim ~~176~~ wherein
2 the first operation code and the data are provided to the memory
3 device via an external bus.

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1 ~~184~~. (previously presented) The method of claim ~~183~~ wherein
2 the external bus includes a set of signal lines used to carry
3 multiplexed address information, the data and control information.

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1 ~~185~~. (previously presented) The method of claim ~~176~~ wherein
2 the second operation code includes precharge information.

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1 ~~186~~. (previously presented) A synchronous memory device,
2 wherein the memory device includes an array of memory cells, the
3 memory device comprises:
4 input receiver circuitry to sample a first operation code in
5 response to a first transition of an external clock signal;
6 a programmable register to store a binary value in response to
7 the first operation code, wherein the binary value is
8 representative of an amount of time to transpire before the memory
9 device outputs data; and
10 output driver circuitry to output data in response to a second
11 operation code and after the amount of time transpires, wherein a
12 first portion of the data is output in response to a second
13 transition of the external clock signal and a second portion of the
14 data is output in response to a third transition of the external
15 clock signal.

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1 ~~187~~. (previously presented) The memory device of claim ~~186~~
2 wherein the binary value is representative of a number of clock
3 cycles of the external clock signal.

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1 ~~188~~. (previously presented) The memory device of claim ~~187~~
2 wherein the second transition of the external clock signal is a
3 rising edge transition and the third transition of the external
4 clock signal is a falling edge transition.

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1 ³⁹~~189~~. (previously presented) The memory device of claim ³⁸~~188~~
2 wherein the second and third transitions of the external clock
3 signal are consecutive transitions.

1 ⁴⁰~~190~~. (previously presented) The memory device of claim ³⁹~~189~~
2 wherein the first operation code and the binary value are included
3 in a packet.

1 ⁴¹~~191~~. (previously presented) The memory device of claim ⁴⁰~~190~~
2 wherein the first operation code and the binary value are included
3 in the same packet.

1 ⁴²~~192~~. (previously presented) The memory device of claim ³⁶~~186~~
2 further including delay lock loop circuitry to generate a first
3 internal clock signal, wherein the data is output in response to
4 the first internal clock signal.

1 ⁴³~~193~~. (previously presented) The memory device of claim ³⁶~~186~~
2 wherein the input receiver circuitry receives address information.

1 ⁴⁴~~194~~. (previously presented) The memory device of claim ³⁶~~186~~
2 wherein the output driver circuitry outputs the data onto an
3 external bus having a set of signal lines used to carry multiplexed
4 address information, the data and control information.

1 ⁴⁵~~185~~. (previously presented) The memory device of claim ⁴⁴~~184~~
2 wherein the input receiver circuitry samples the first operation
3 code from the external bus.

1 ⁴⁶~~186~~. (previously presented) The memory device of claim ³⁶~~186~~
2 wherein the output driver circuitry and the input receiver
3 circuitry are connected to a common pad.

1 ⁴⁷~~187~~. (previously presented) The memory device of claim ³⁶~~186~~
2 wherein the memory device is a synchronous dynamic random access
3 memory.

1 ⁴⁸~~198~~. (previously presented) A synchronous memory device
2 including an array of memory cells, wherein the memory device
3 comprises:

4 a programmable register to store a binary value;

5 a plurality of input receivers to sample first and second
6 operation codes synchronously with respect to an external clock
7 signal, wherein:

8 the first operation code initiates storage of the binary
9 value in the programmable register; and

10 the second operation code initiates a read operation; and
11 a plurality of output drivers to output data in response to
12 the second operation code, wherein:

13 a first portion of the data is output synchronously with
14 respect to a rising edge transition of the external clock
15 signal; and

16 a second portion of the data is output synchronously with
17 respect to a falling edge transition of the external clock
18 signal.

1 ⁴⁹~~199~~. (previously presented) The memory device of claim ⁴⁸~~198~~
2 wherein the first operation code is sampled synchronously with
3 respect to a first transition of the external clock signal and the
4 second operation code is sampled synchronously with respect to a
5 second transition of the external clock signal.

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1 ~~200~~. (previously presented) The memory device of claim ~~199~~ 49
2 wherein the first operation code is included in a control register
3 access packet and the second operation code is included in a read
4 request packet.

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1 ~~201~~. (previously presented) The memory device of claim ~~200~~ 50
2 wherein the read request packet includes address information.

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1 ~~202~~. (previously presented) The memory device of claim ~~198~~ 48
2 wherein the array of memory cells includes dynamic memory cells.

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1 ~~203~~. (previously presented) The memory device of claim ~~202~~ 52
2 wherein the memory device further includes a delay lock loop,
3 coupled to the plurality of output drivers, to synchronize the
4 outputting of data with the external clock signal.

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1 ~~204~~. (previously presented) The memory device of claim ~~203~~ 53
2 wherein the delay lock loop further includes:
3 a delay line to generate an internal clock signal, wherein the
4 internal clock signal has a delay with respect to the external
5 clock signal; and
6 a comparator to compare the internal clock signal with the
7 external clock signal, wherein the delay of the internal clock
8 signal is adjusted based on the comparison between the internal
9 clock signal and the external clock signal.

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1 ⁵⁵~~205~~. (previously presented) The memory device of claim ⁴⁸~~198~~
2 wherein the second operation code includes precharge information.

1 ⁵⁶~~206~~. (previously presented) The memory device of claim ⁵⁵~~205~~
2 further including a plurality of sense amplifiers to access the
3 data from the array of memory cells, wherein the precharge
4 information initiates automatic precharge of the plurality of sense
5 amplifiers after the data is accessed from the array of memory
6 cells.

1 ⁵⁷~~207~~. (previously presented) The memory device of claim ⁴⁸~~198~~
2 wherein the binary value represents a device identifier.

1 ⁵⁸~~208~~. (previously presented) The memory device of claim ⁴⁸~~198~~
2 wherein the binary value represents a location of a defective
3 portion of the array of memory cells.

1 ⁵⁹~~209~~. (previously presented) The memory device of claim ⁴⁸~~198~~
2 wherein the binary value represents a delay time.

1 ⁶⁰~~210~~. (currently amended) The memory device of claim ⁵⁹~~209~~ ~~198~~
2 wherein the first portion of data is output, in response to the
3 second operation code, after the delay time transpires.